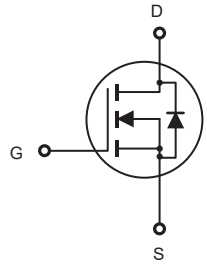
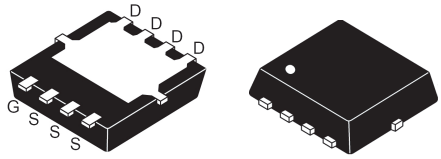
CEZC4112A

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 40V, 40A, $R_{DS(ON)}$ = 10.2 mΩ @V_{GS} = 10V.
  $R_{DS(ON)}$ = 16 mΩ @V_{GS} = 4.5V.
- Super High dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.





P-PAK 3X3

ABSOLUTE MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D@$R_{\theta Jc}$	40	A
	I_D@$R_{\theta JA}$	12	A
Drain Current-Pulsed [a]	I_{DM}@$R_{\theta Jc}$	160	A
	I_{DM}@$R_{\theta JA}$	48	A
Maximum Power Dissipation	P_D	25	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case [b]	$R_{\theta Jc}$	5	°C/W
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	50	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D =10A		8.2	10.2	mΩ
		V_{GS} = 4.5V, I_D =8A		10	16	mΩ
Dynamic Characteristics [c]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		1220		pF
Output Capacitance	C_{oss}			150		pF
Reverse Transfer Capacitance	C_{rss}			115		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 32V, I_D = 10A, V_{GS}= 10V, R_{GEN}= 6Ω		22		ns
Turn-On Rise Time	t_r			13		ns
Turn-Off Delay Time	$t_{d(off)}$			61		ns
Turn-Off Fall Time	t_f			13		ns
Total Gate Charge	Q_g	V_{DS} = 32V, I_D = 10A, V_{GS} = 4.5V		14.6		nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			9.7		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				20	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = 15A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

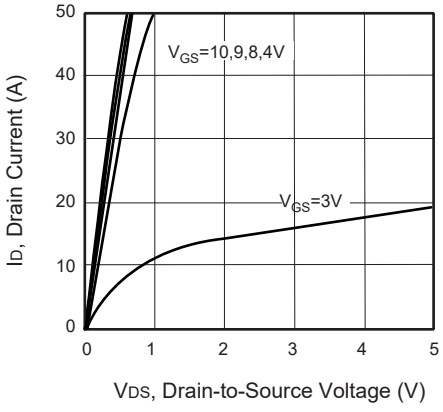


Figure 1. Output Characteristics

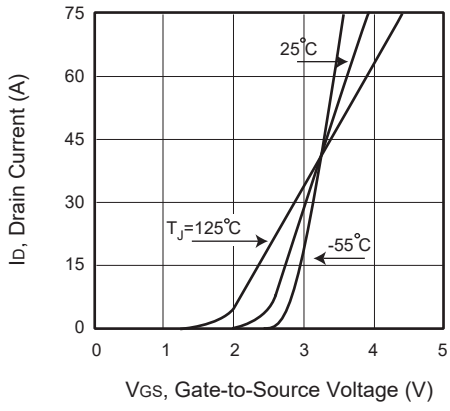


Figure 2. Transfer Characteristics

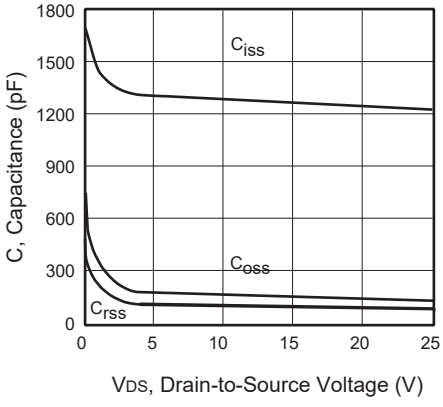


Figure 3. Capacitance

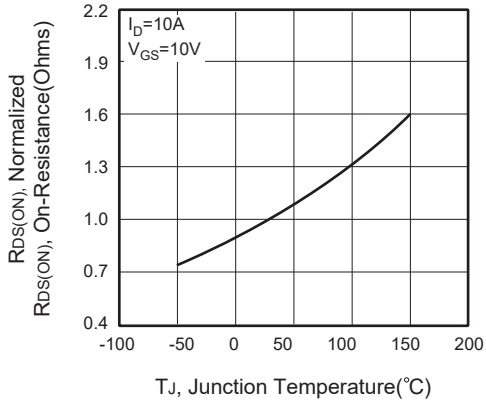


Figure 4. On-Resistance Variation with Temperature

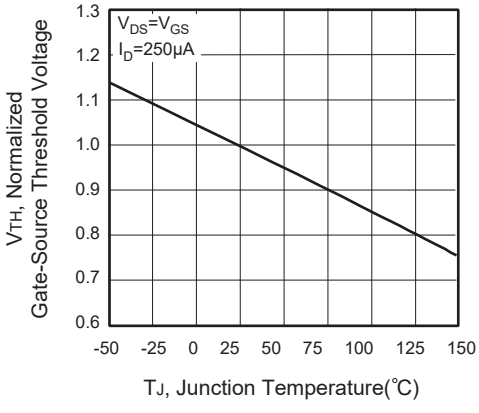


Figure 5. Gate Threshold Variation with Temperature

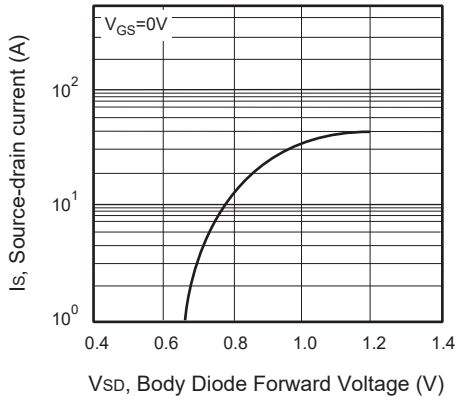


Figure 6. Body Diode Forward Voltage Variation with Source Current

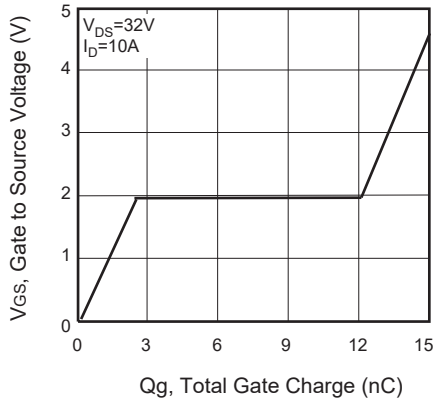


Figure 7. Gate Charge

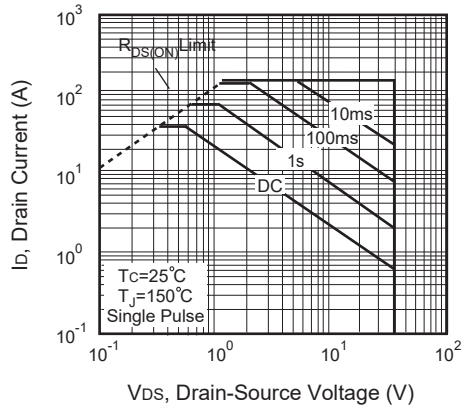


Figure 8. Maximum Safe Operating Area

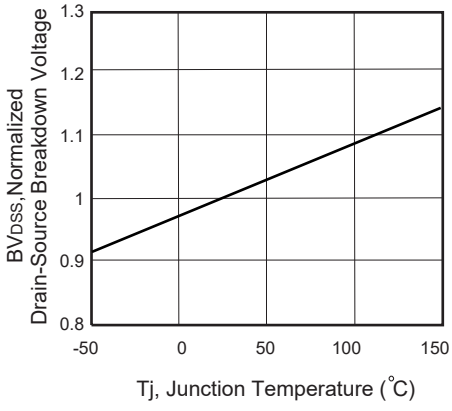


Figure 9. Breakdown Voltage Variation VS Temperature

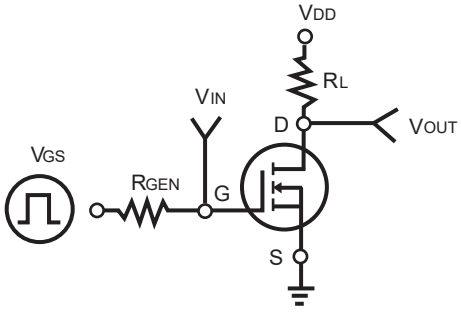


Figure 10. Switching Test Circuit

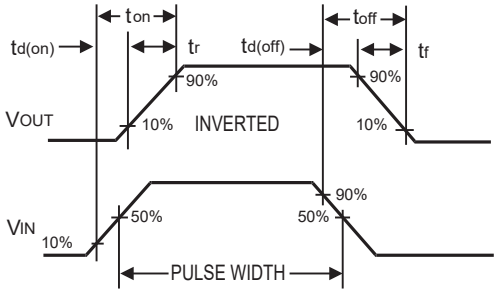


Figure 11. Switching Waveforms

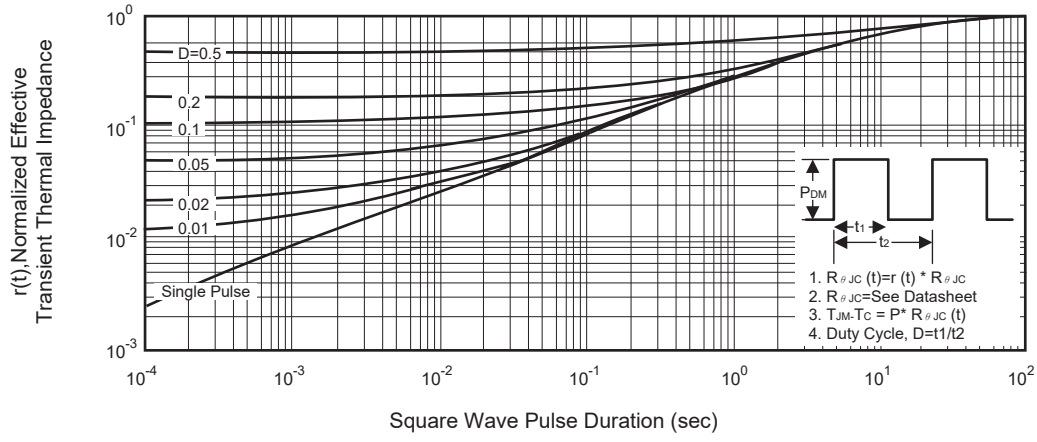
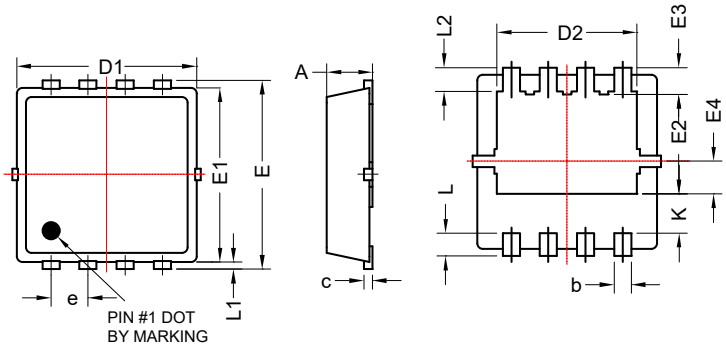
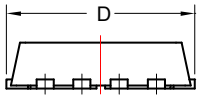


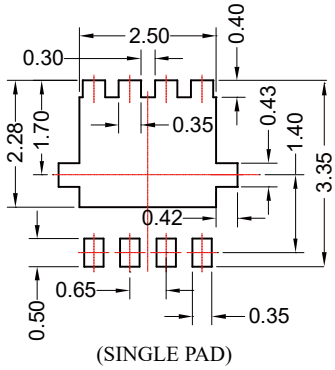
Figure 12. Normalized Thermal Transient Impedance Curve

P-PAK 3X3 產品外觀尺寸圖 (Product Outline Dimension)

SINGLE PAD 尺寸圖







(SINGLE PAD)

(Lead Pattern Recommendation)

SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.7	0.85	0.028	0.033
b	0.20	0.40	0.008	0.016
c	0.10	0.25	0.004	0.010
D	3.15	3.45	0.124	0.136
D1	3.00	3.25	0.118	0.128
D2	2.29	2.65	0.090	0.104
E	3.15	3.45	0.124	0.136
E1	2.90	3.20	0.114	0.126
E2	1.54	1.94	0.061	0.076
E3	0.28	0.65	0.011	0.026
E4	0.37	0.77	0.015	0.030
e	0.65(BSC)		0.026(BSC)	
K	0.50	0.89	0.02	0.035
L	0.30	0.50	0.012	0.020
L1	0.06	0.20	0.002	0.008
L2	0.27	0.57	0.011	0.022